

Figure 1

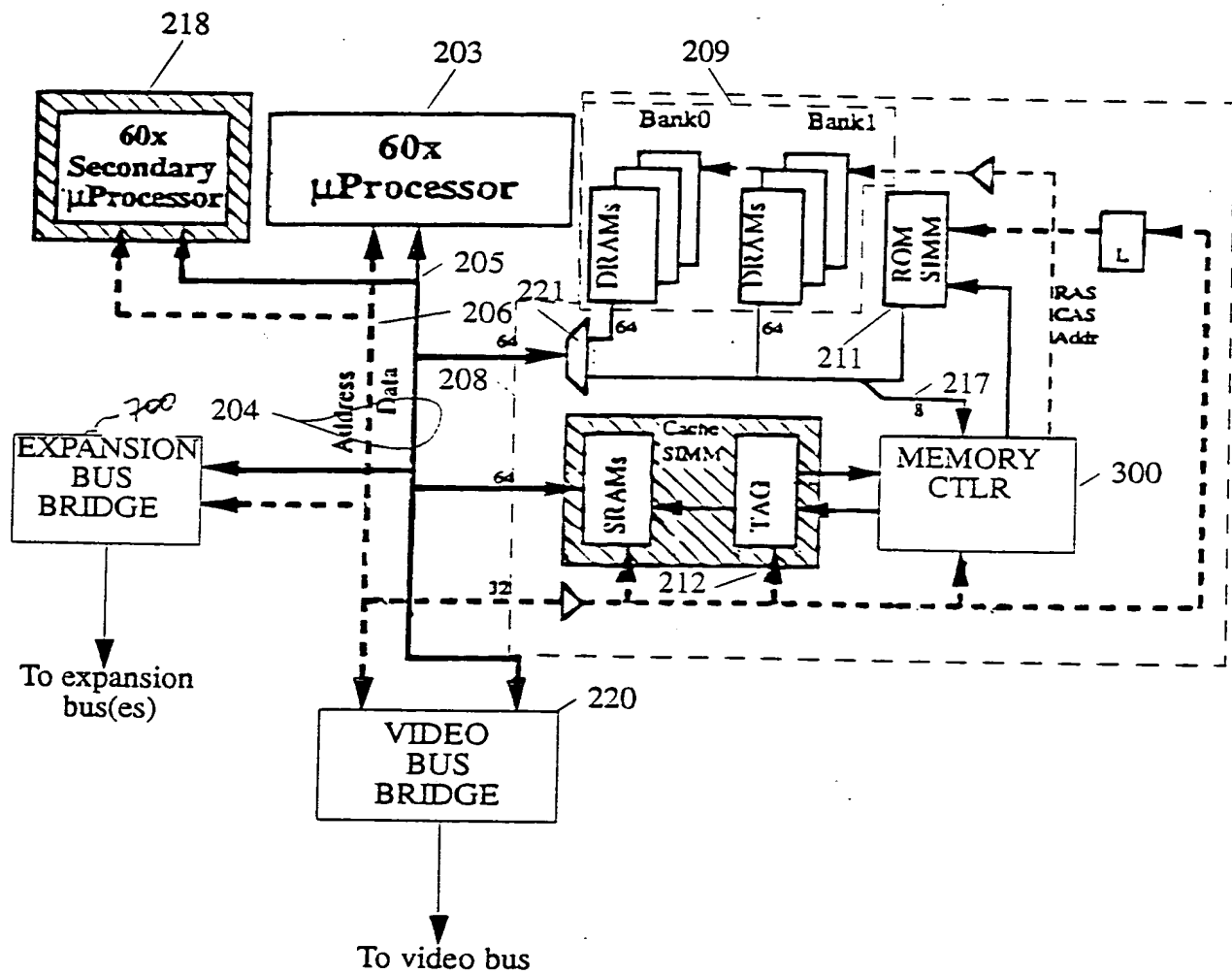


Figure 2

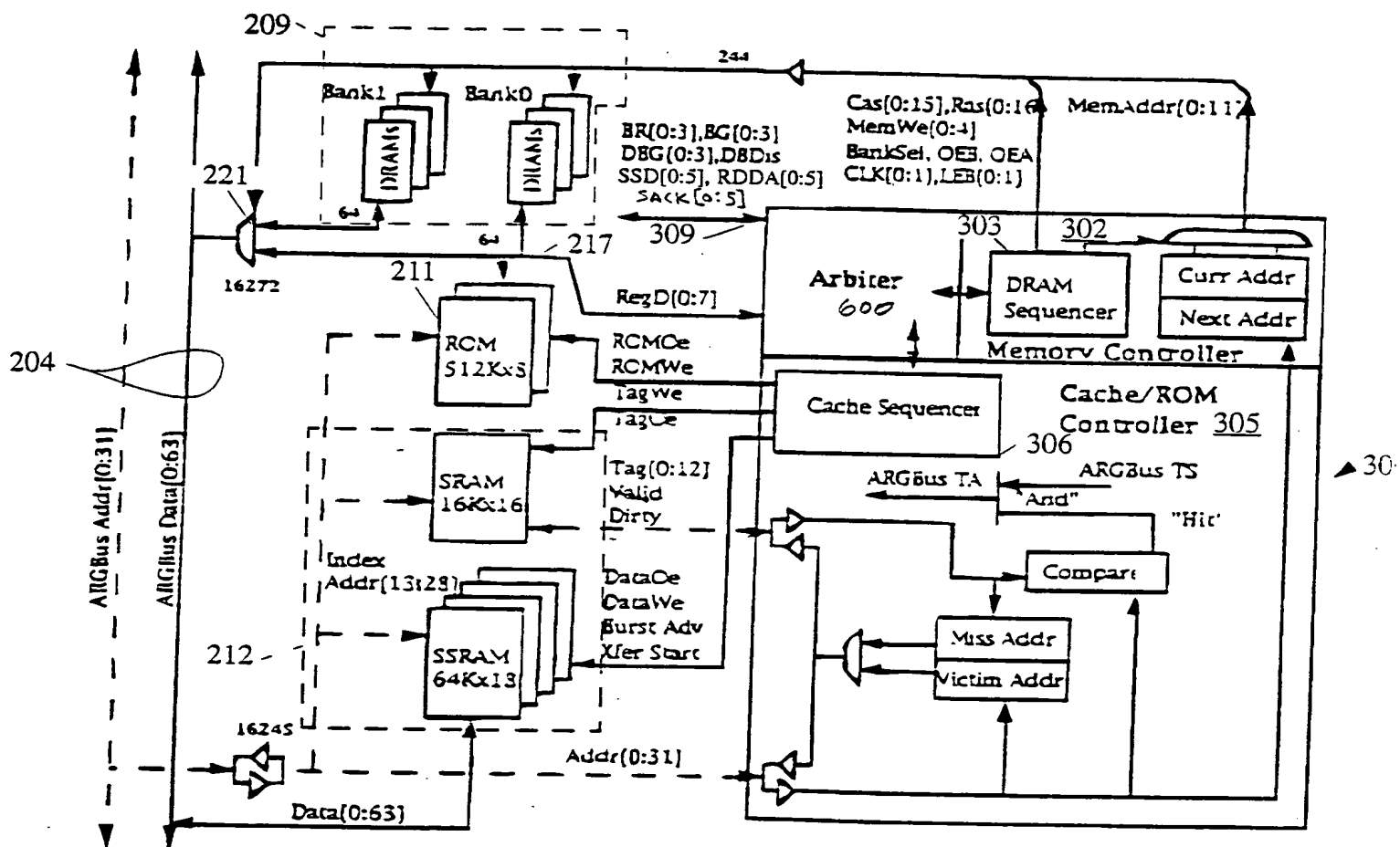
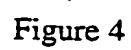


Figure 3



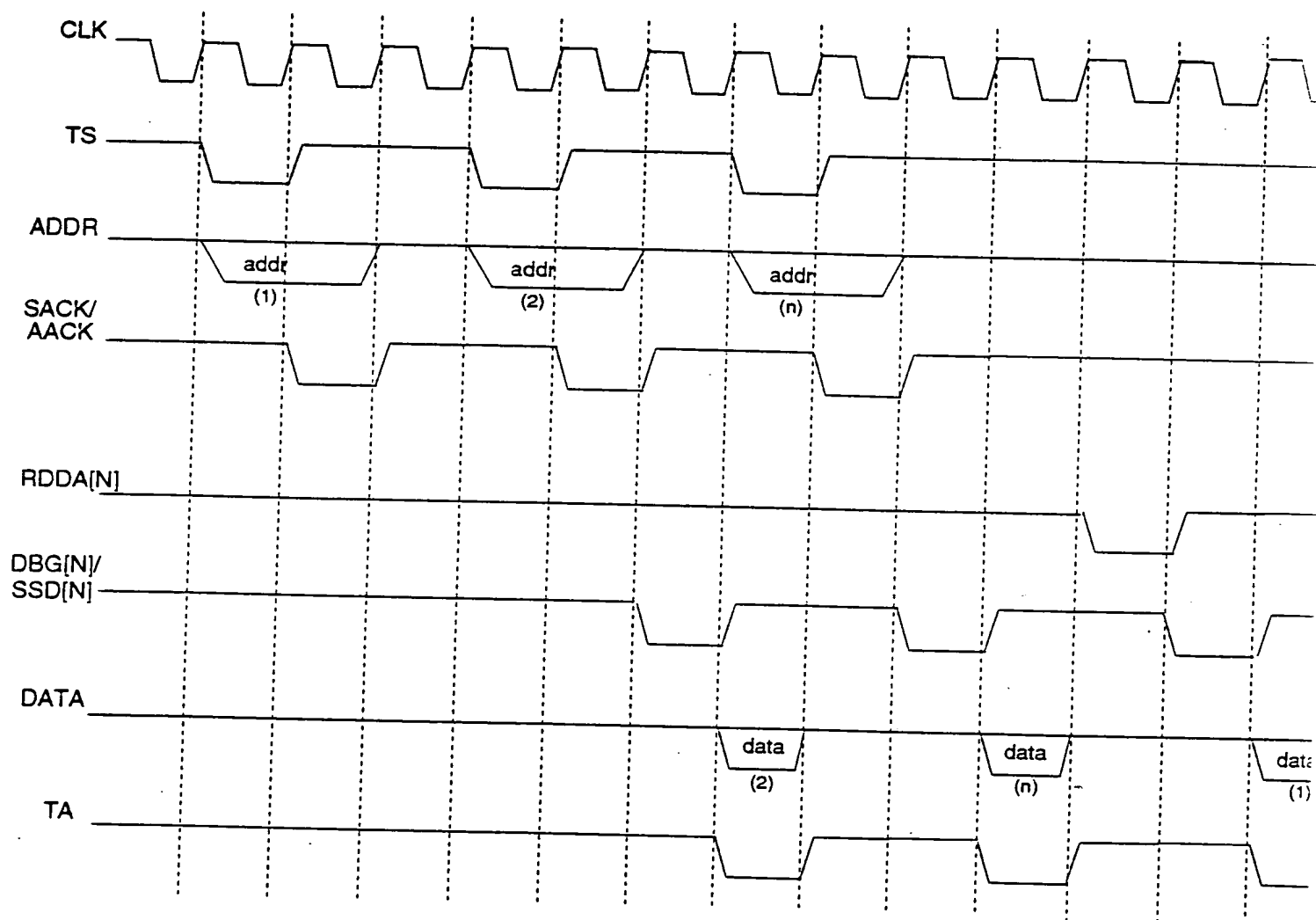


Figure 5

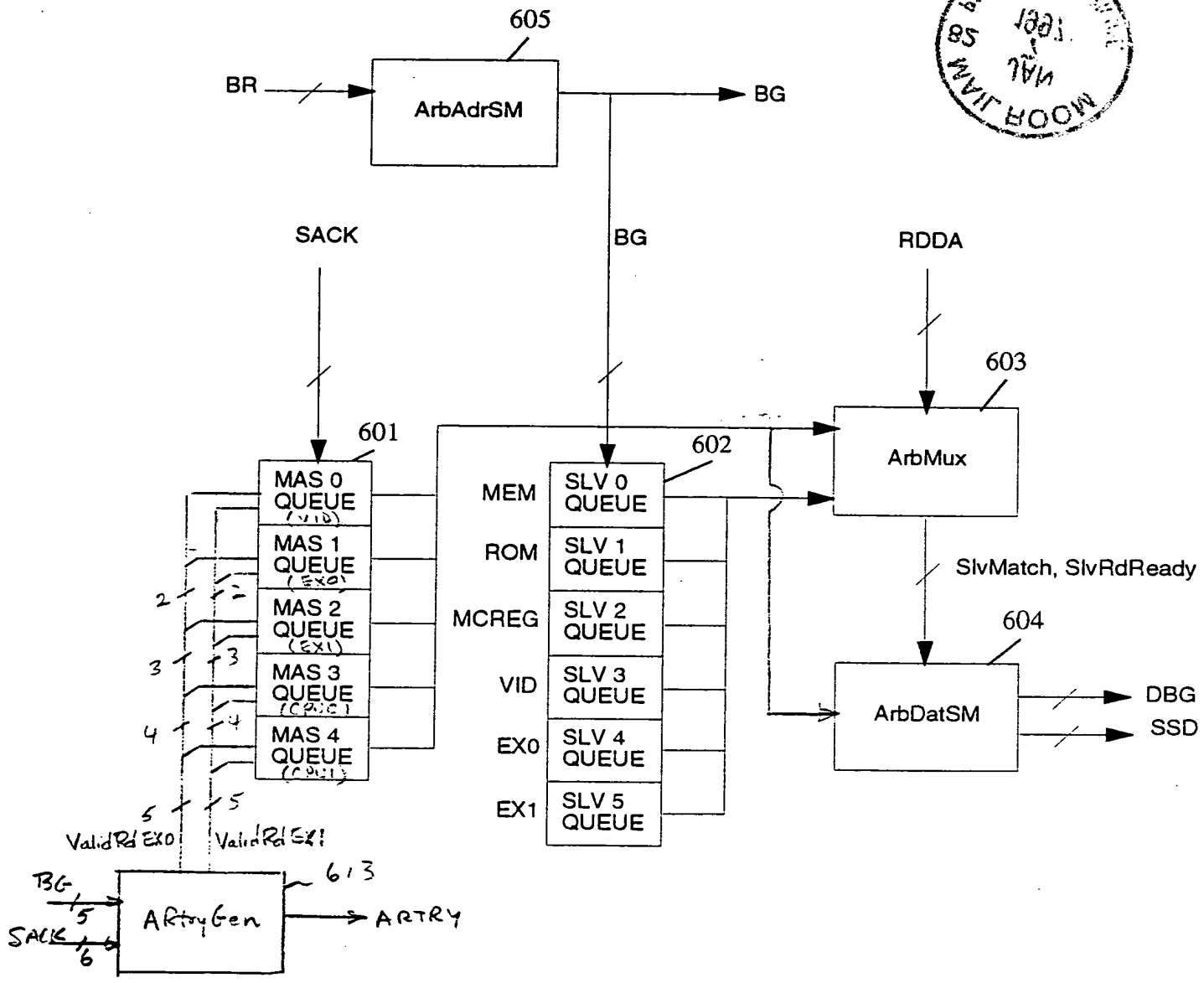


Figure 6

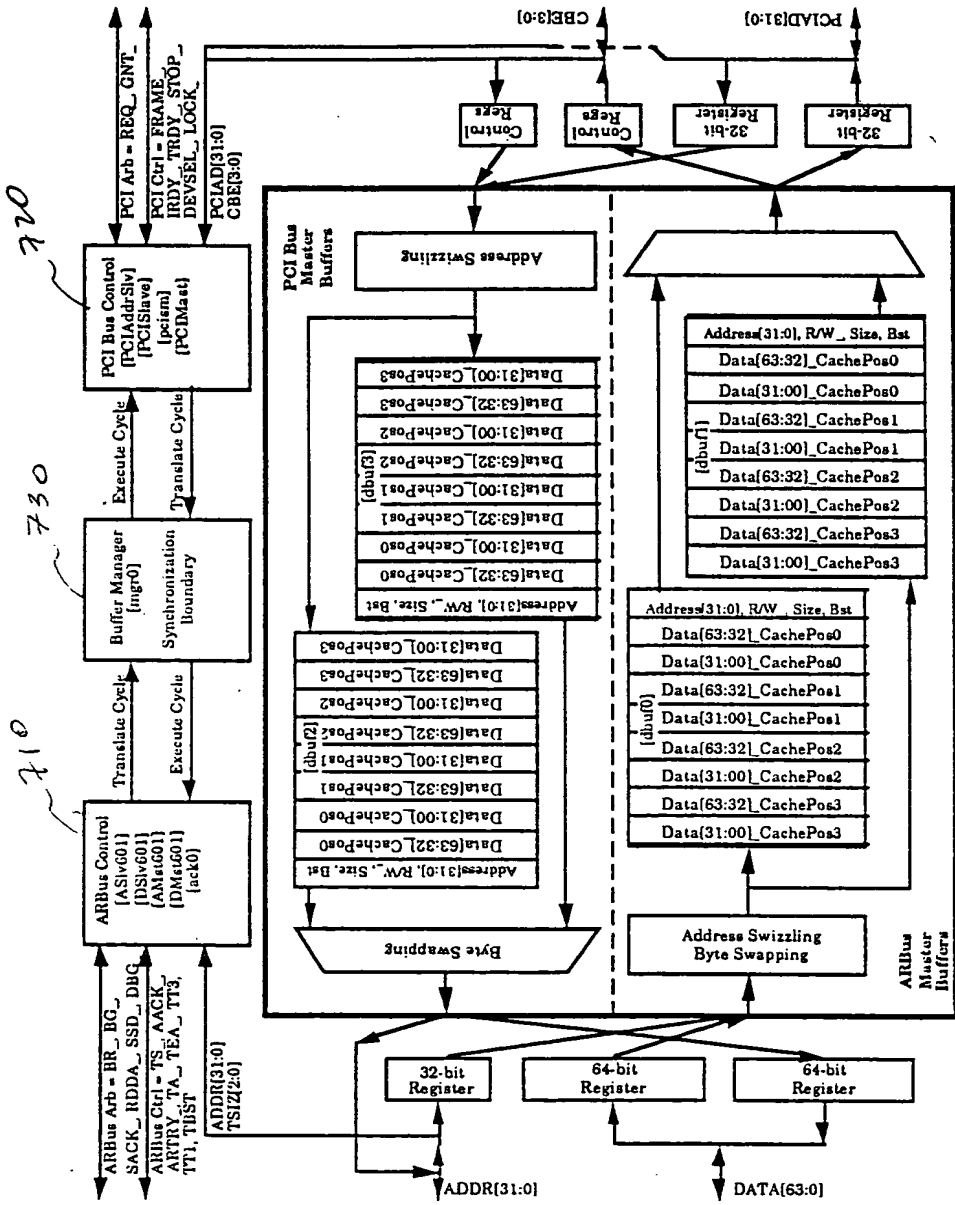


Fig 7

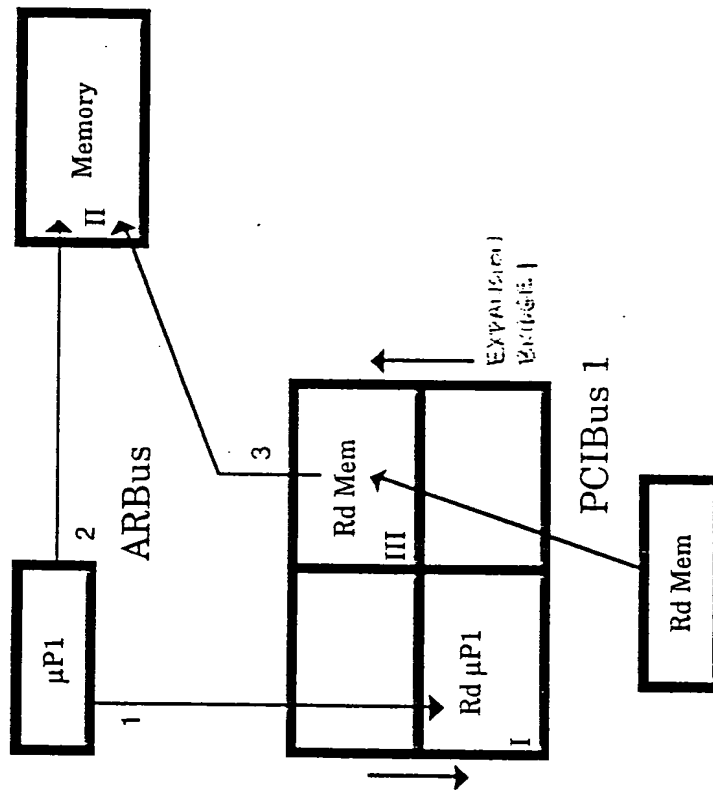


Fig 2

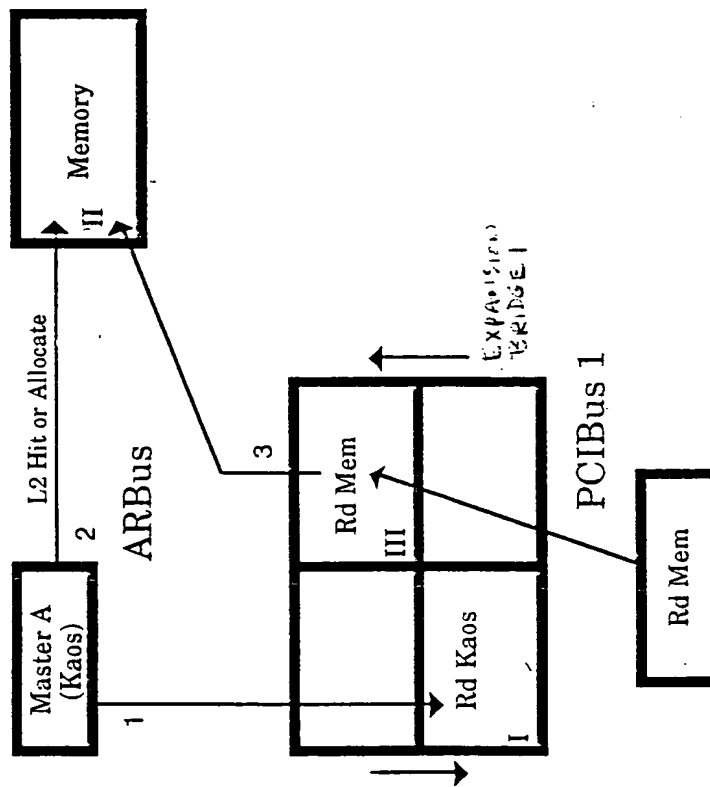


Fig 9

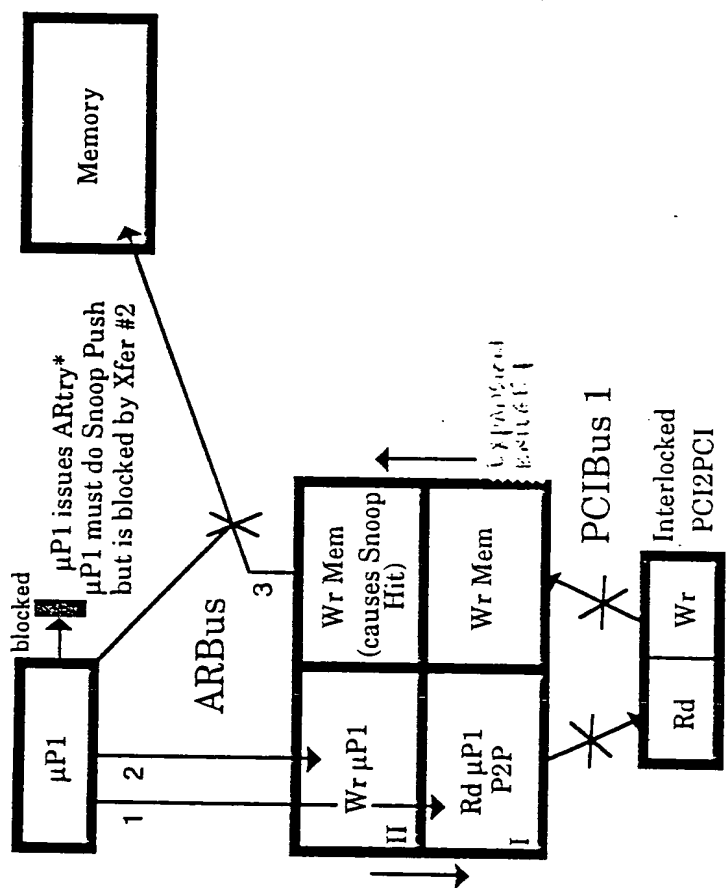


Fig 10



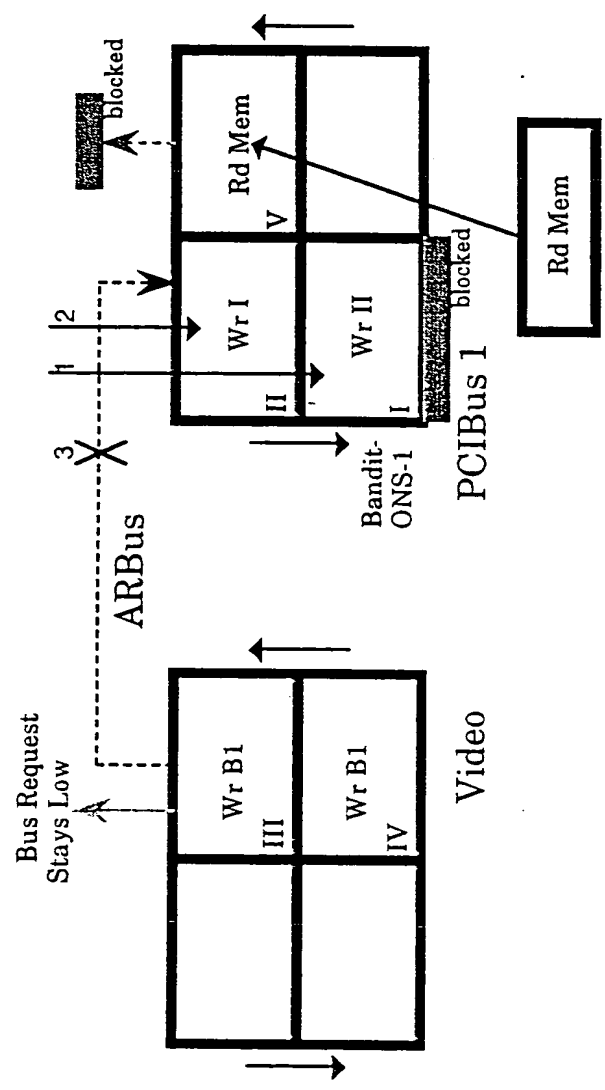
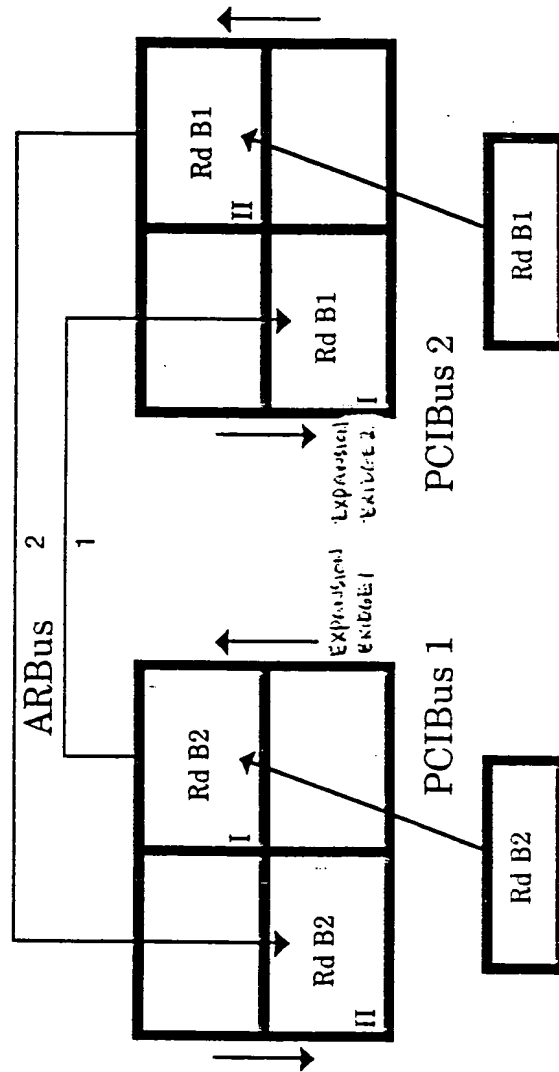
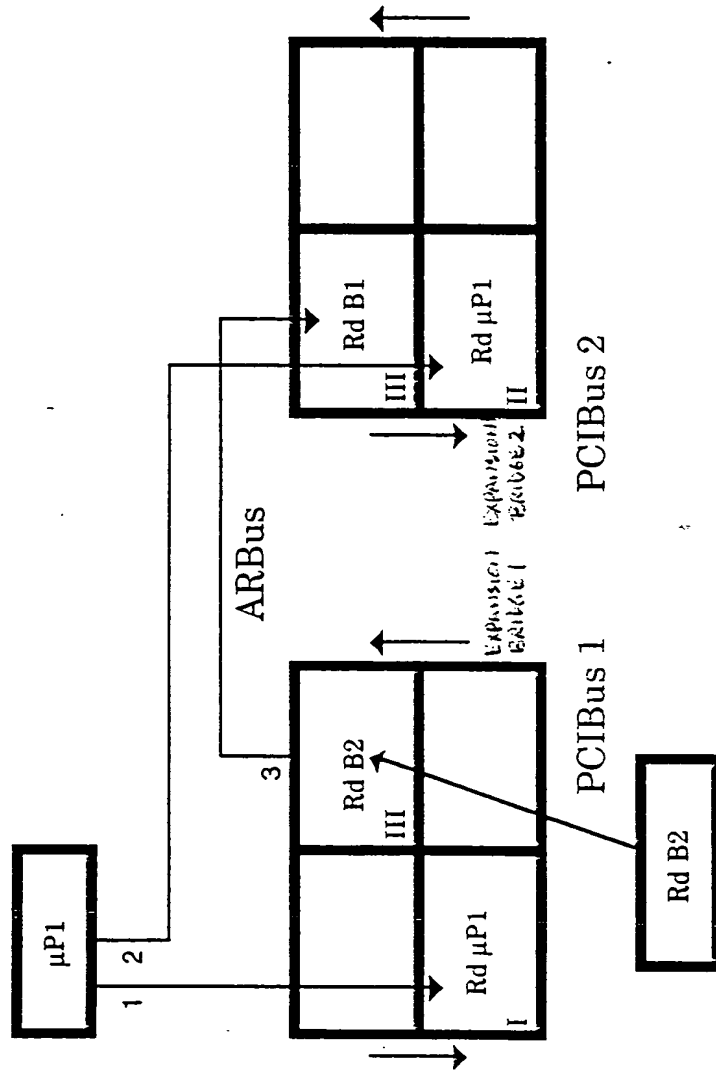


Fig 12



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7-10-14

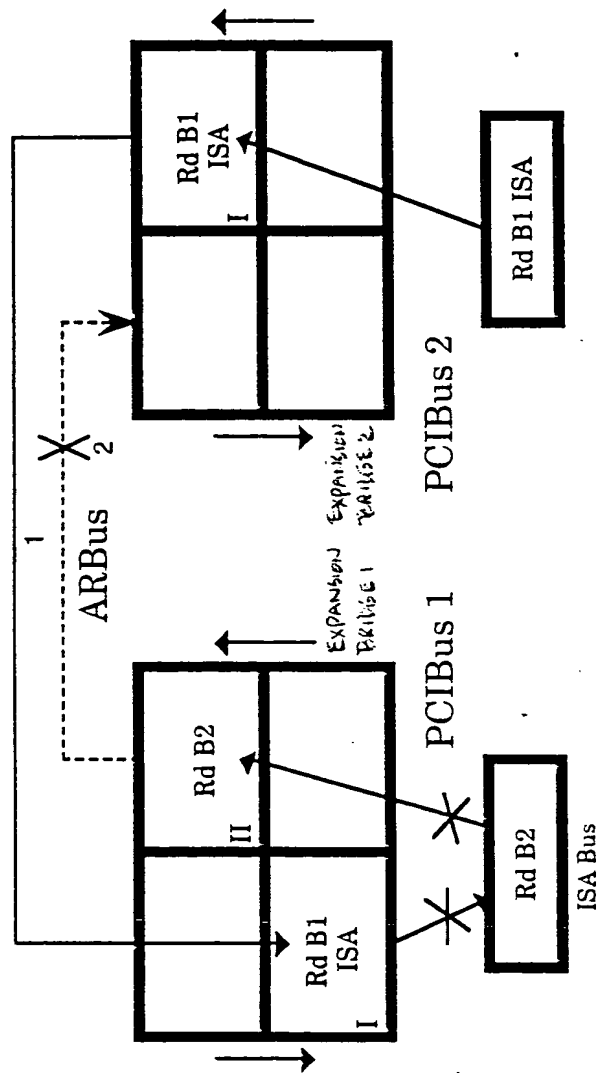


Fig 15

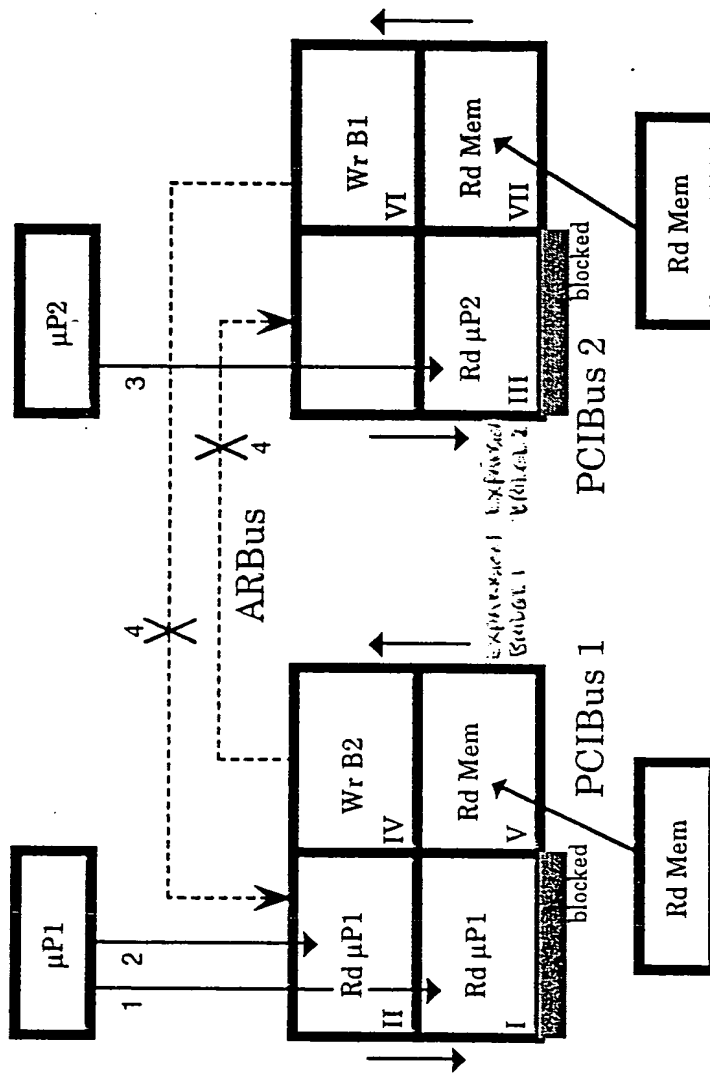


FIG 16



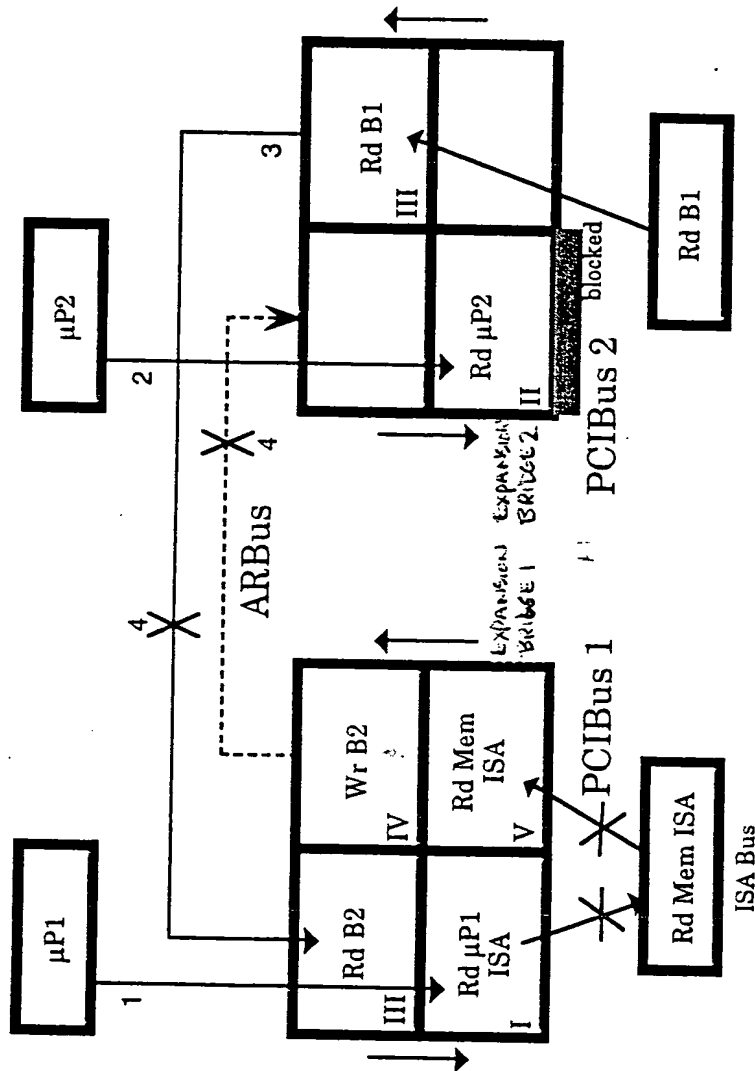
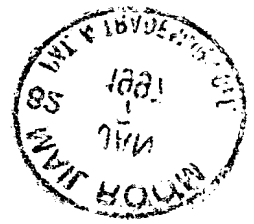


Fig 17

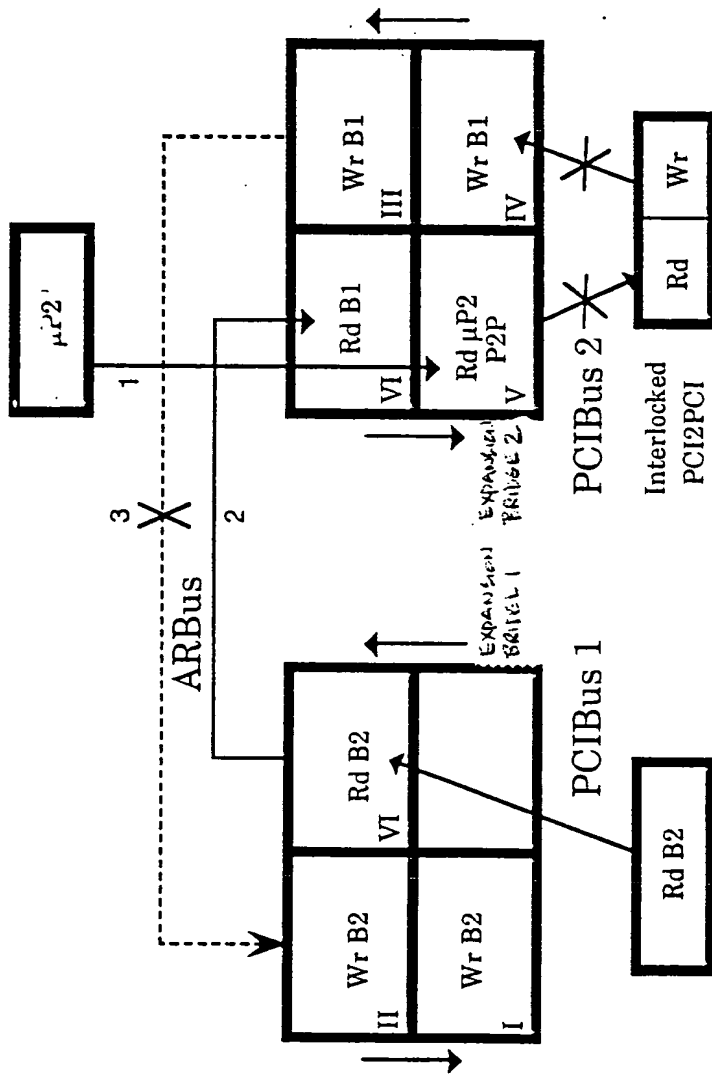
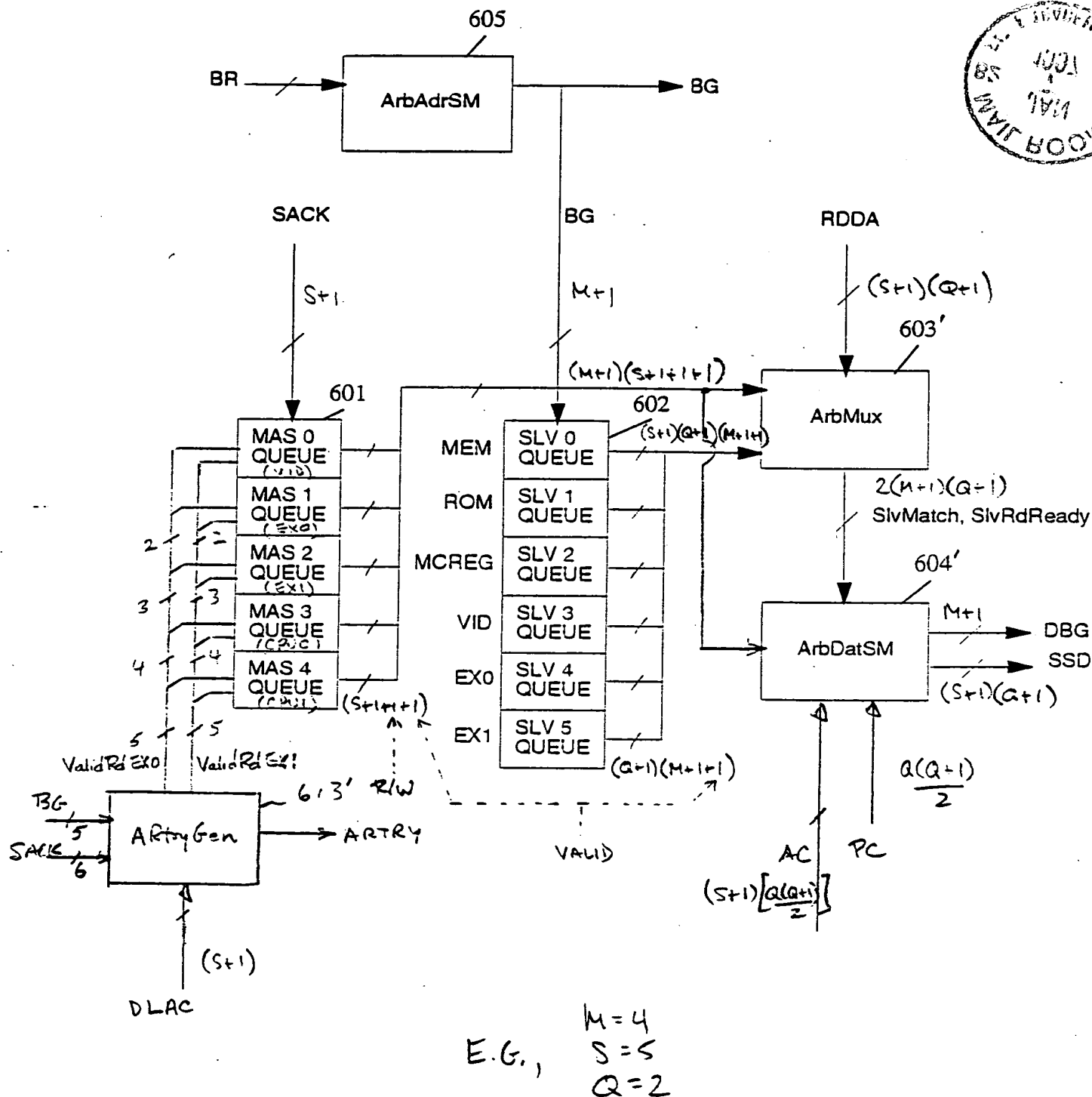


Fig. 18





19  
Figure 6

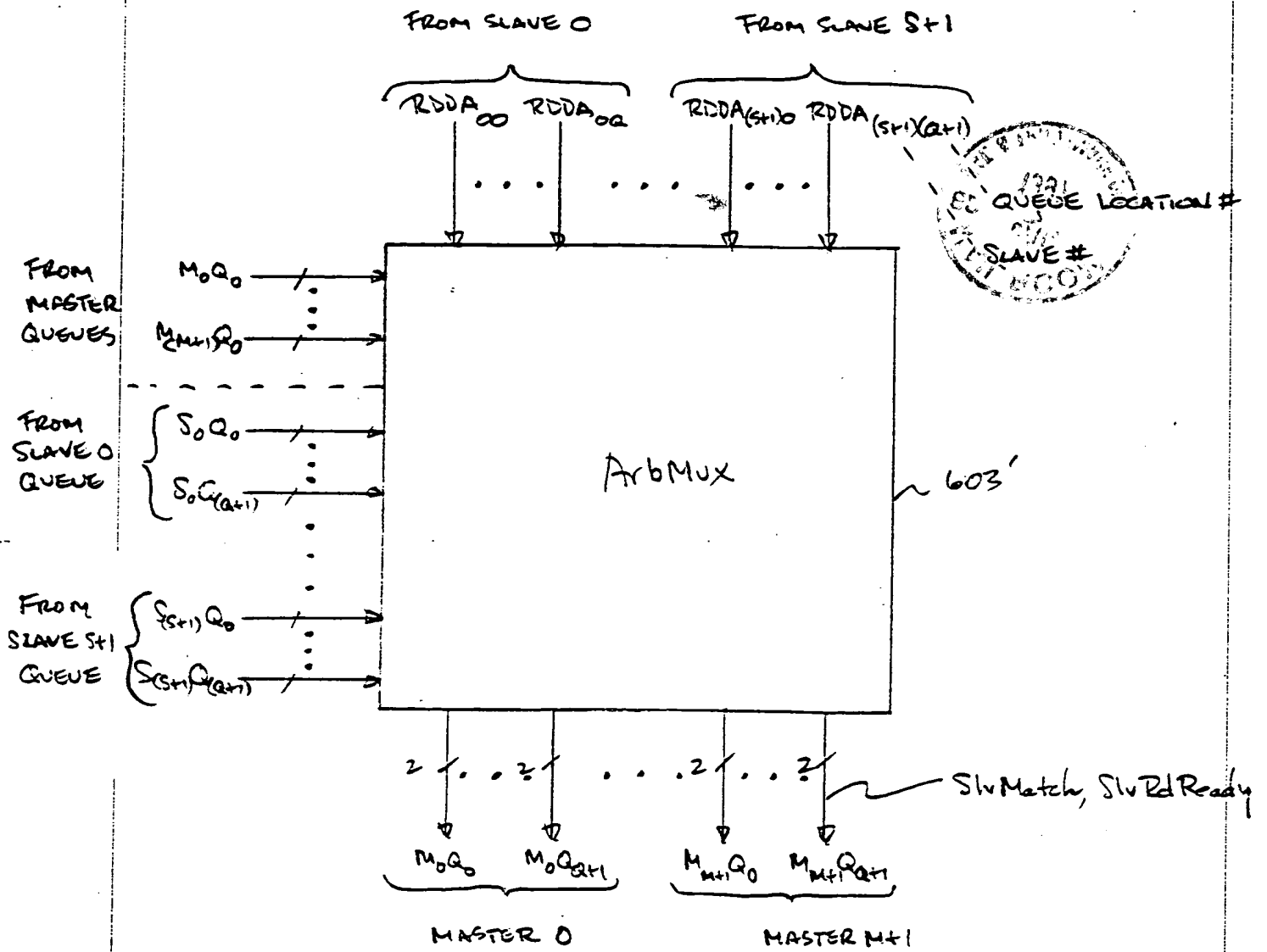


FIG. 20

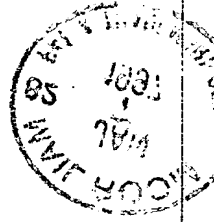
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 R4DA 40 41 42  
 R5DA 50 51 52

M0Q0 8  
 M1Q0 8  
 M2Q0 8  
 M3Q0 8  
 M4Q0 8  
 S0Q0 6  
 S0Q1 6  
 S0Q2 6  
 S1Q0 6  
 S1Q1 6  
 S1Q2 6  
 S2Q0 6  
 S2Q1 6  
 S2Q2 6  
 S3Q0 6  
 S3Q1 6  
 S3Q2 6  
 S4Q0 6  
 S4Q1 6  
 S4Q2 6  
 S5Q0 6  
 S5Q1 6  
 S5Q2 6

Fig 21

~603'

ArbMux



SlvMatch, SlvRdReady

M0Q0 M0Q1 M0Q2 M1Q0 M1Q1 M1Q2 M2Q0 M2Q1 M2Q2 M3Q0 M3Q1 M3Q2 M4Q0 M4Q1 M4Q2 M5Q0 M5Q1 M5Q2

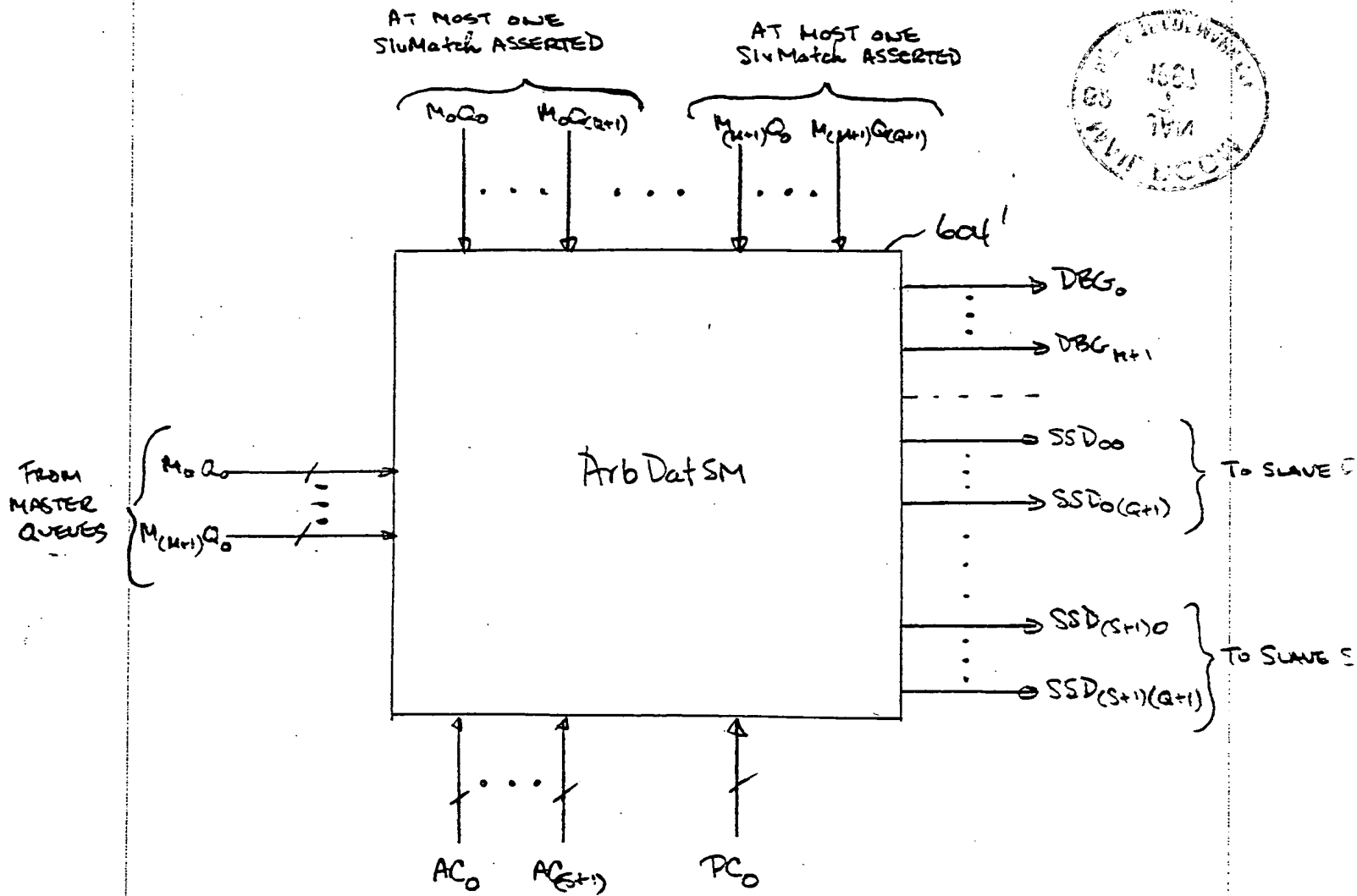


Fig 22

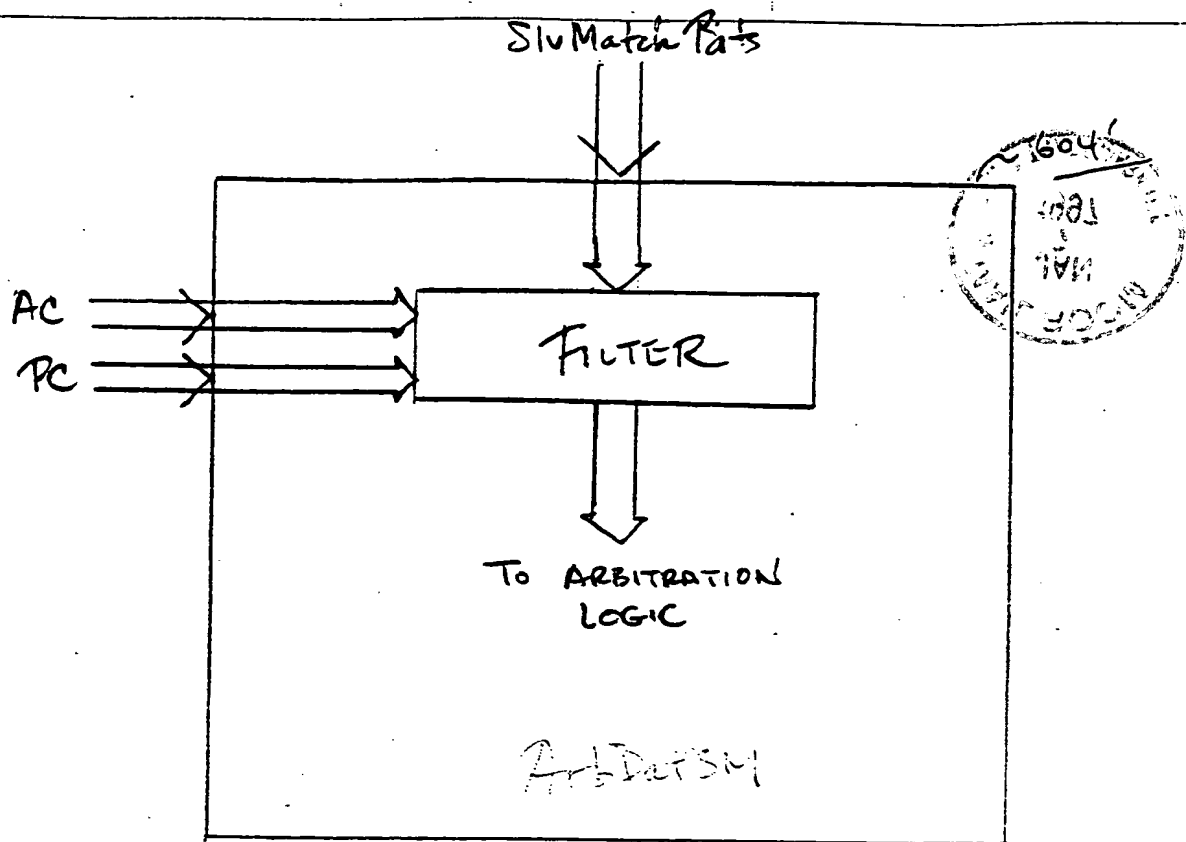


Fig 23

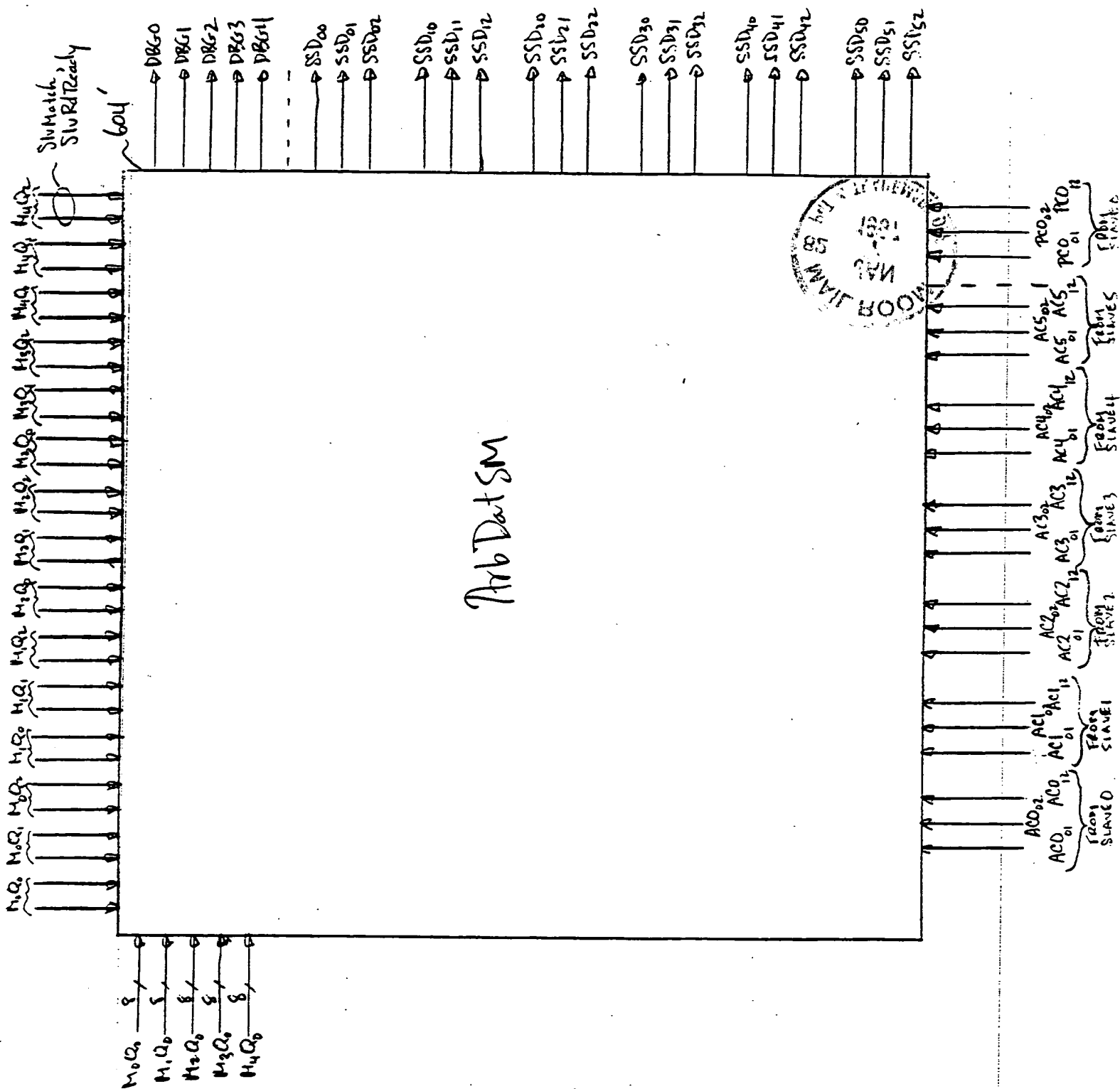


Fig 24

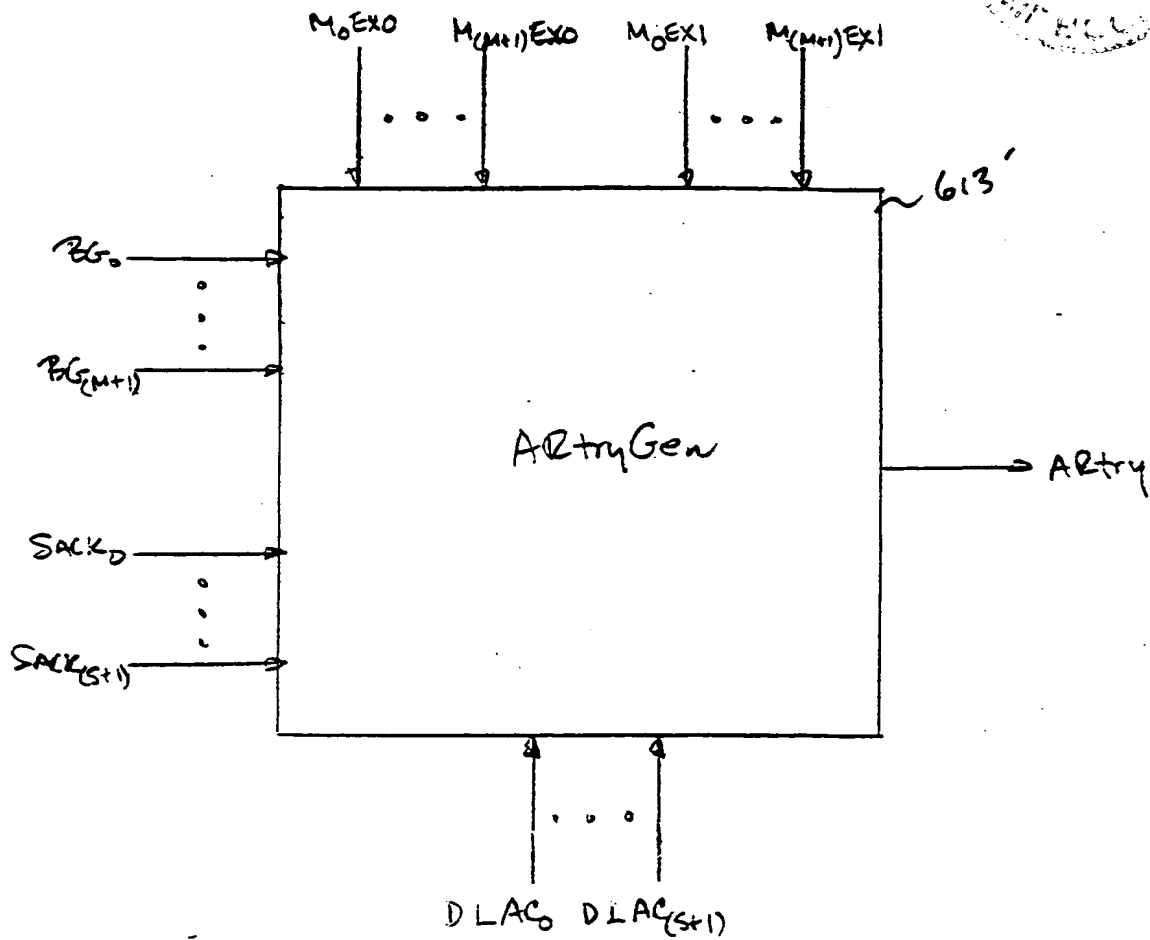


Fig 25

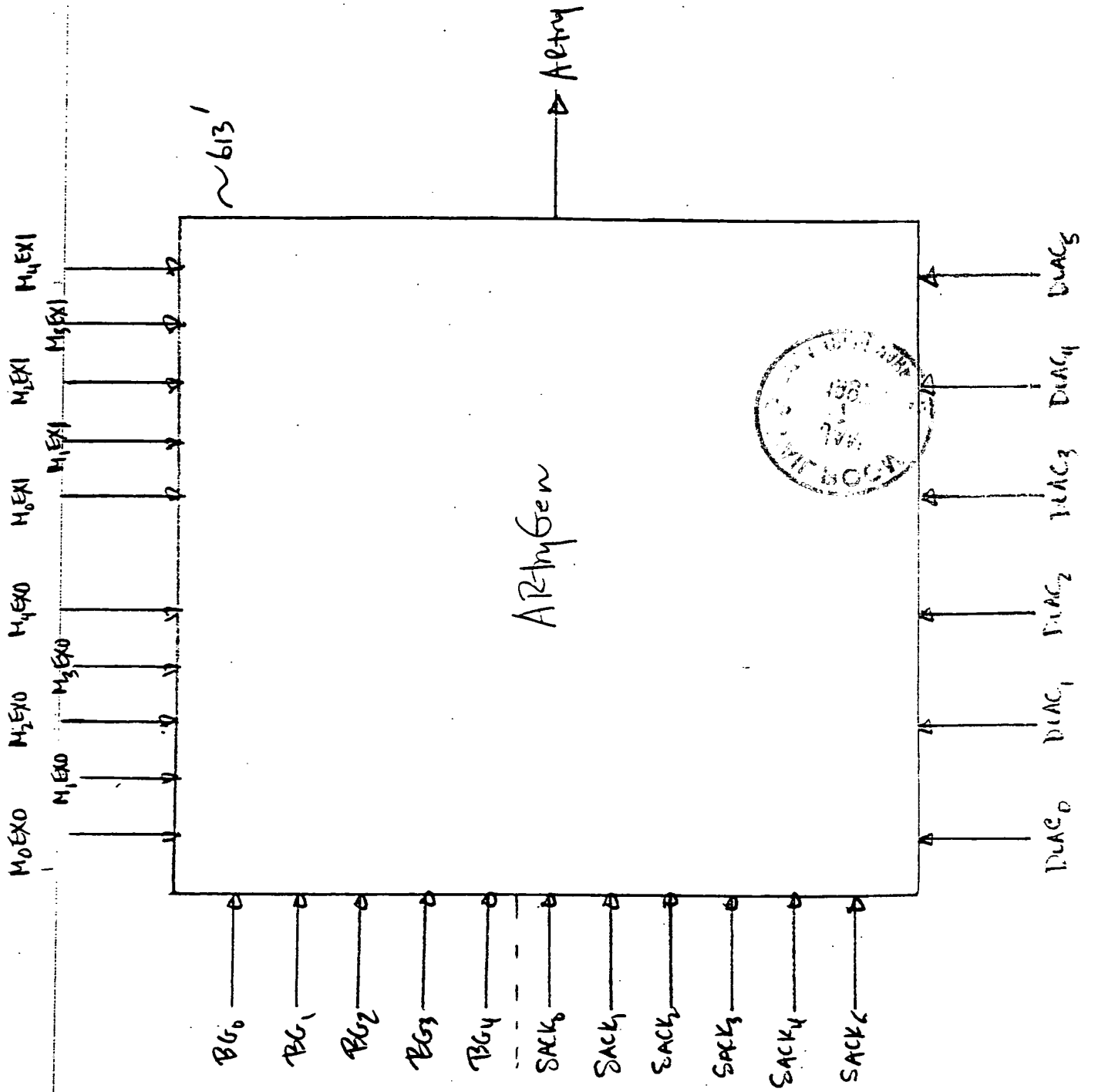


Fig 26